IN THE CLAIMS

1. (Currently Amended) A method of coupling a semiconductor die with a next level package, comprising:

providing at least one interconnect;

arranging the semiconductor die, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package;

generating an electromagnetic flux with an inductor; and

exposing the semiconductor die to the electromagnetic flux to preferentially induce eddy currents in the semiconductor die to heat the semiconductor die and couple the semiconductor die with the next level package.

2. (Currently Amended) The method of claim 1, ~~wherein the heating preferentially heats the semiconductor die over the next level package.~~ wherein preferentially inducing eddy currents in the semiconductor die is achieved by modulating the frequency of an alternating current such that the at least one interconnect and the next level package is not induced with eddy currents.

3. (Original) The method of claim 2, wherein generating an electromagnetic flux comprises providing an alternating electric current having a frequency exceeding 1 megahertz.

4. (Original) The method of claim 3, wherein generating an electromagnetic flux comprises providing an alternating electric current having a frequency of approximately 13.2 megahertz.

5. (Original) The method of claim 3, wherein the at least one interconnect comprises an array of interconnects.

6. (Original) The method of claim 5, wherein the array of interconnects is formed on the semiconductor die.

7. (Original) The method of claim 6, further comprising arranging the inductor such that the semiconductor die is interposed between the inductor and the next level package.

8. (Original) The method of claim 7, wherein the next level package is a substrate.

9. (Original) The method of claim 8, wherein the next level package is a flexible substrate.

10. (Original) The method of claim 7, wherein the next level package is an interposer.

11. (Original) The method of claim 7, wherein the next level package is a printed wiring board.

12. (Original) The method of claim 6, further comprising arranging the inductor such that the next level package is interposed between the inductor and the semiconductor die.

13. (Original) The method of claim 12, wherein the next level package is a substrate.

14. (Original) The method of claim 13, wherein the next level package is a flexible substrate.

15. (Original) The method of claim 12, wherein the next level package is an interposer.

16. (Original) The method of claim 12, wherein the next level package is a printed wiring board.

17. (Currently Amended) A method of coupling a semiconductor die with a next level package, comprising:

providing at least one interconnect;

arranging the semiconductor die, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package;

generating an electromagnetic flux with an inductor; and

exposing the at least one interconnect to the electromagnetic flux to preferentially induce eddy currents in the at least one interconnect to heat the at least one interconnect and couple the semiconductor die with the next level package.

18. (Currently Amended) The method of claim 17, ~~wherein the heating preferentially heats the at least one interconnect over the at least one next level package.~~ wherein preferentially inducing eddy currents in the at least one interconnect is achieved by modulating the frequency of an alternating current such that the semiconductor die and the next level package is not induced with eddy currents.

19. (Original) The method of claim 18, wherein the heating preferentially heats the at least one interconnect over the semiconductor die.

20. (Original) The method of claim 19, wherein generating an electromagnetic flux comprises providing an alternating electric current having a frequency exceeding 1 megahertz.

21. (Original) The method of claim 20, wherein generating an electromagnetic flux comprises providing an alternating electric current having a frequency of approximately 13.2 megahertz.

22. (Original) The method of claim 20, wherein the at least one interconnect comprises an array of interconnects.

23. (Original) The method of claim 22, wherein the array of interconnects is formed on the semiconductor die.

24. (Original) The method of claim 23, further comprising arranging the inductor such that the semiconductor die is interposed between the inductor and the next level package.

25. (Original) The method of claim 24, wherein the next level package is a substrate.

26. (Original) The method of claim 25, wherein the next level package is a flexible substrate.

27. (Original) The method of claim 24, wherein the next level package is an interposer.

28. (Original The method of claim 24, wherein the next level package is a printed wiring board.

29. (Original) The method of claim 23, further comprising arranging the inductor such that the next level package is interposed between the inductor and the semiconductor die.

30. (Original) The method of claim 29, wherein the next level package is a substrate.

31. (Original) The method of claim 30, wherein the next level package is a flexible substrate.

32. (Original) The method of claim 29, wherein the next level package is an interposer.

33. (Original) The method of claim 29, wherein the next level package is a printed wiring board.

34. (Previously Presented) The method of claim 1, wherein exposing the semiconductor die to the electromagnetic flux to induce eddy currents in the semiconductor die comprises scanning the inductor around the semiconductor die.

35. (Previously Presented) The method of claim 1, wherein exposing the semiconductor die to the electromagnetic flux to induce eddy currents in the semiconductor die comprises scanning a pancake coil inductor around the semiconductor die.

36. (Previously Presented) The method of claim 17, wherein exposing the at least one interconnect to the electromagnetic flux to induce eddy currents in the at least one interconnect comprises scanning the inductor around the semiconductor die.

37. (Previously Presented) The method of claim 17, wherein exposing the at least one interconnect to the electromagnetic flux to induce eddy currents in the at least one interconnect comprises scanning a pancake coil inductor around the at least one interconnect.

38. (Previously Presented) A method of coupling a semiconductor die with a next level package comprising:

providing at least one interconnect;

arranging the semiconductor die, the next level package, and the at least

one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package;

generating an electromagnetic flux with a pancake coil;

exposing the semiconductor die to the electromagnetic flux to induce heating in the semiconductor die; and

heating the semiconductor die to couple the semiconductor die with the next level package.

39. (Previously Presented) The method of claim 38, wherein
the electromagnetic flux induces eddy currents in the semiconductor die.

40. (Previously Presented) The method of claim 38, wherein
the pancake coil inductor is scanned around the semiconductor die.

41. (Previously Presented) A method of coupling a semiconductor die with a next level package, comprising:

providing at least one interconnect;

arranging the semiconductor die, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package;

generating an electromagnetic flux with an inductor;

scanning the inductor around the semiconductor die while generating an electromagnetic flux;

exposing the semiconductor die to the electromagnetic flux to induce heating in the semiconductor die; and

heating the semiconductor die to couple the semiconductor die with the next level package.

42. (Previously Presented) The method of claim 41, wherein
the inductor is a pancake coil inductor.

43. (Previously Presented) The method of claim 41, wherein
the electromagnetic flux induces eddy currents in the semiconductor die.

44. (Previously Presented) A method of coupling a semiconductor die with a next level package comprising:

providing at least one interconnect;

arranging the semiconductor die, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package;

generating an electromagnetic flux with a pancake coil;

exposing the at least one interconnect to the electromagnetic flux to induce heating in the at least one interconnect; and

heating the at least one interconnect to couple the semiconductor die with the next level package.

45. (Previously Presented) The method of claim 44, wherein
the electromagnetic flux induces eddy currents in the at least one interconnect.

46. (Previously Presented) The method of claim 44, wherein
the pancake coil inductor is scanned around the at least one interconnect.

47. (Previously Presented) A method of coupling a semiconductor die with a next level package, comprising:

providing at least one interconnect;

arranging the semiconductor die, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package;

generating an electromagnetic flux with an inductor;

scanning the inductor around the at least one interconnect while generating an electromagnetic flux;

exposing the at least one interconnect to the electromagnetic flux to induce heating in the at least one interconnect; and

heating the at least one interconnect to couple the semiconductor die with the next level package.

48. (Previously Presented) The method of claim 47 wherein the inductor is a pancake coil inductor.

49. (Previously Presented) The method of claim 47, wherein the electromagnetic flux induces eddy currents in the at least one interconnect.